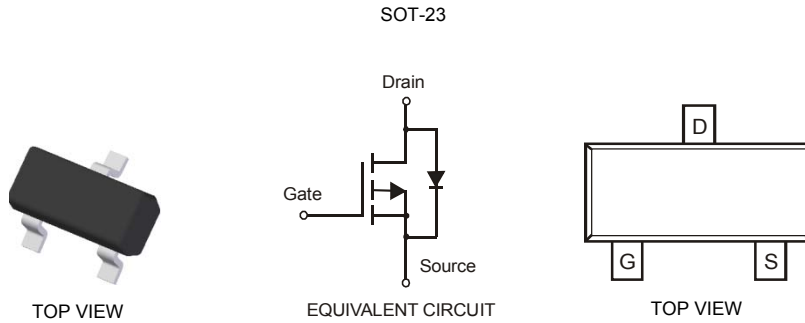


Features

- Low On-Resistance:
 - $R_{DS(ON)} < 100m\Omega$ @ $V_{GS} = -4.5V$, $I_D = -2.7A$
 - $R_{DS(ON)} < 215m\Omega$ @ $V_{GS} = -2.5V$, $I_D = -2.0A$
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT-23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

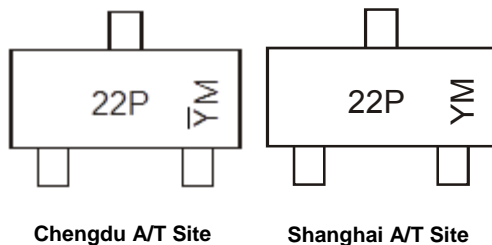


Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2215L-7	SOT-23	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

Marking Information



22P = Product Type Marking Code
 YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 ȲM = Date Code Marking for CAT (Chengdu Assembly/ Test site)
 Y or Ȳ = Year (ex: A = 2013)
 M = Month (ex: 9 = September)

Date Code Key

Year	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
Code	U	V	W	X	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V _{DSS}	-20	V
Gate-Source Voltage			V _{GSS}	±12	V
Drain Current (Note 5)	Steady State	T _A = 25°C T _A = 70°C	I _D	-2.7 -2	A
Pulsed Drain Current (Note 6)			I _{DM}	8	A

Thermal Characteristics

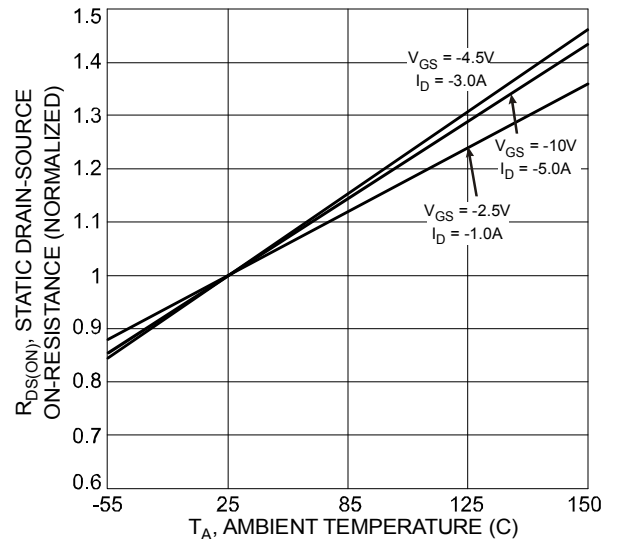
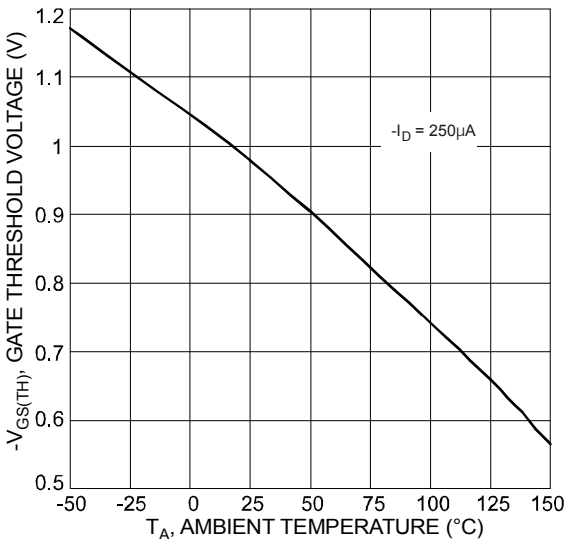
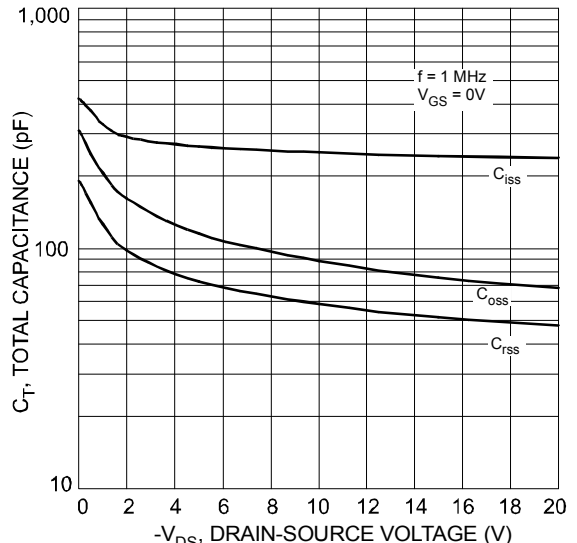
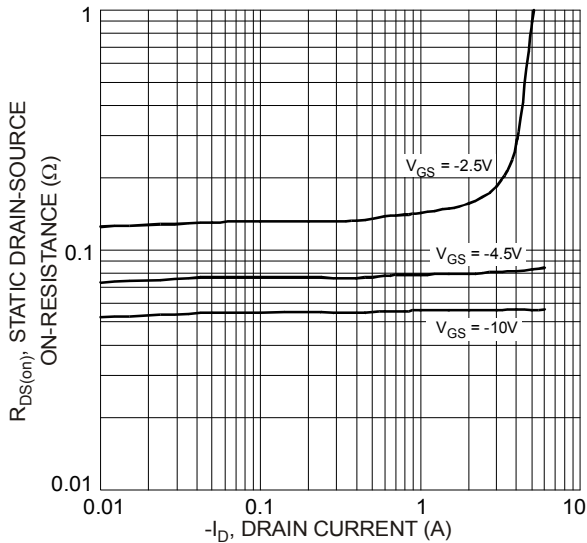
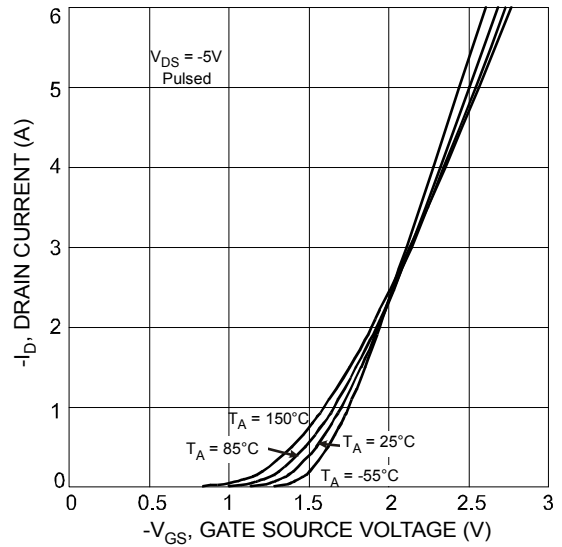
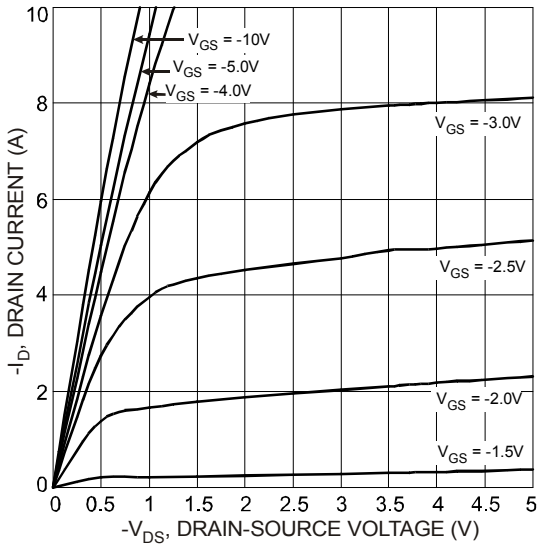
Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P _D	1.08	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 5)	R _{θJA}	115	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PCB. t ≤ 5 sec.
6. Pulse width ≤ 10μs, Duty Cycle ≤ 1%.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-20	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-800	nA	V _{DS} = -20V, V _{GS} = 0V
On-State Drain Current	I _{D(ON)}	-6	—	—	A	V _{DS} ≤ -5V, V _{GS} = -4.5V
		-3	—	—		V _{DS} ≤ -5V, V _{GS} = -2.5V
Gate-Source Leakage	I _{GSS}	—	—	±80	nA	V _{GS} = ±12V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	-0.45	—	-1.25	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	80	100	mΩ	V _{GS} = -4.5V, I _D = -2.7A
		—	165	215		V _{GS} = -2.5V, I _D = -2.0A
Forward Transfer Admittance	Y _{fs}	—	4	—	S	V _{DS} = -5V, I _D = -2.7A
Diode Forward Voltage (Note 7)	V _{SD}	—	—	-1.26	V	V _{GS} = 0V, I _S = -2.7A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	250	—	pF	V _{DS} = -10V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	—	88	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	58	—	pF	
Gate Resistance	R _g	—	12	16	Ω	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	4.3	5.3	nC	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -2.7A
Gate-Source Charge	Q _{gs}	—	0.9	—		
Gate-Drain Charge	Q _{gd}	—	2.1	—		

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.



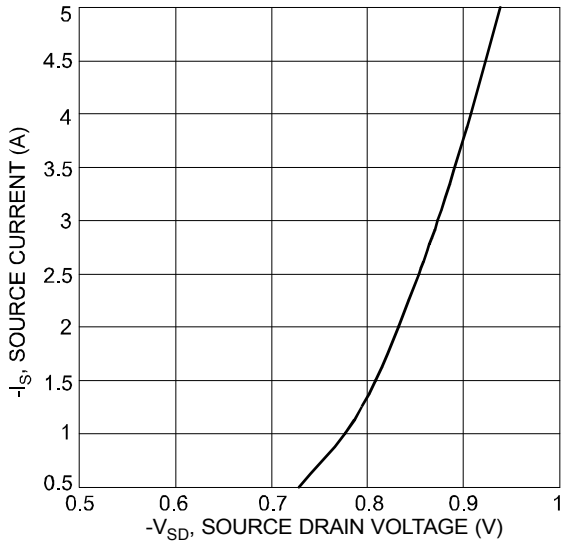
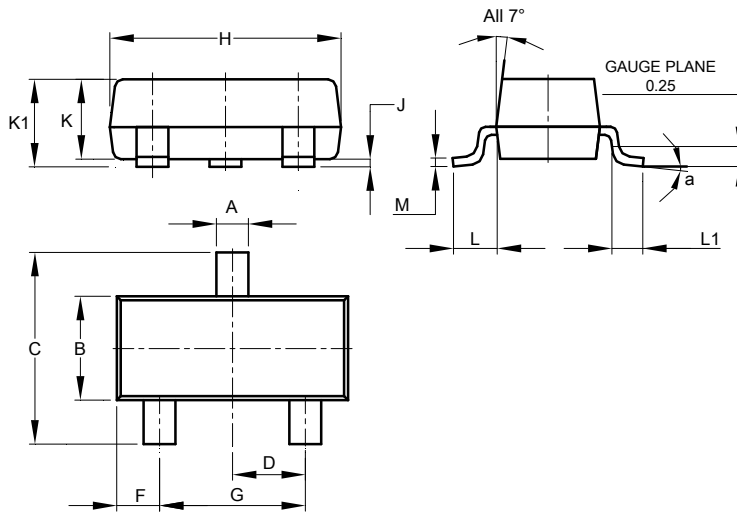


Fig. 7 Reverse Drain Current vs. Source-Drain Voltage

Package Outline Dimensions

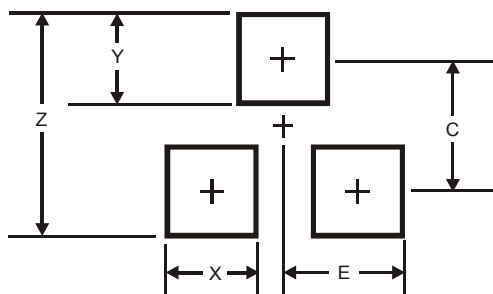
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
α	8°		
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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